geminix SIL4 platform and our design services boost the development of your safety critical applications
Who we are

NEAT is an independent, privately held, Italian design and development company, with extensive experience in creating exclusive hardware and software solutions for mission and safety critical applications, offering highly specialized engineering services for clients who play a major role in avionics, aerospace, railway, military and industrial markets.

In addition, NEAT provides its own 2oo2 HW/SW SIL4-assessed Intellectual Property, GeminiX, a HW/SW platform enabling the implementation of safety-critical and/or high reliability embedded applications, certifiable with levels of safety integrity up to SIL4.

In 2018, NEAT joined UNIFE.

Know-how

NEAT exploits specific and certifiable design-flows, which respect the strictest criteria required by the safety regulations (CE/IEC SIL - level 4 and DO178C/254 - level A) and the highest quality standards (ISO9001:2015, IRIS, ISO9100:2009). Moreover, NEAT has considerable know-how both in the standard development and in the certification process of railway applications (EN50126/50128/50129/50 155/50159, IEC61508). The products delivered by NEAT assure total reliability even in harsh environments and thus meet the required safety standards.

NEAT has solid, extensive experience in the HW/SW co-design, in the development of real-time S/W applications and in the use of programmable logical devices.

NEAT adopts the most advanced techniques for the simulation, design, development testing and qualification of its products. For example, specific tools are used to perform: Model Driven Design, Design for Testability, Whole System Simulation and Fault Injection Test.

NEAT has developed other tools for Defensive Programming, H/W and S/W Integration Automatic Test, Finite State Machine Verification, Safety-Critical Data Preparation.

NEAT boasts first rate expertise in the development of mission and/or safety-critical algorithms and applications in the following areas: Synthetic Aperture Radar (SAR), UAV piloting, flying and control route optimization, Emergency Management.

Excellence in technical skills:

• Over 18 years of experience in the development of mission and safety critical systems
• More than 65 mission and safety critical projects:
  • 28 railway
  • 18 avionic/space
  • 10 industrial
  • 11 ICT
• Entirely developed by NEAT:
  • 1,800,000 C/C++ SLOC
  • 610,000 C#/VB SLOC
  • 310,000 VHDL SLOC
  • 275,000 test cases
  • 1,600 documents
  • 76 different custom boards (with production kit)
• Other specific expertise:
  • Development of multi-supplier interoperable data preparation tools (ERTMS/SCMT)
  • Integration of EN50159 compliant protocols (026, 038, 037, 058/056/057/PROFIBUS, 108, PVS), CIP EtherNet/IP™
  • “ERTMS/ECTS; On-line Key Management FFFIS” Subset-137 compliant protocol released as an open-source library (www.kmc-subset137.eu)
Capabilities

Design services
NEAT offers its expertise in the design and development of digital, CPU based electronic boards and systems mostly targeted for safety critical contexts: requirements collection, architectural design, system design, schematic entry, board layout, backplanes, enclosures, FPGA code (VHDL), software libraries, applications and software tools development.

Fast prototyping and production
For system production, NEAT has selected and qualified several international electronic and mechanical manufacturing services from among the market leaders.

For systems fast prototyping, NEAT exploits some internal facilities: pick and place machine, BGA reworking station, optical BGA inspection tool, reflow oven, pre-compliance type testing (thermal, EMI/EMC, insulation). Other dedicated tools complete the list of the internal laboratory: serial data analyzer, oscilloscopes, meters and a climate chamber.

Single boards computer databases
NEAT designs and develops custom and semi-custom computer systems and releases the complete design kit to its clients. Our job is focused on computers for safety-critical applications and on high-availability redundant computers (commonly used in railways and avionic applications). Wherever the application and the environment give critical constraints with respect to safety, performances, power consumption, size and whenever a custom design is mandatory, NEAT can play a crucial role.

Our computers use the most advanced and performing CPUs on the market, such as Multicore ARM® V8-64b, PowerPC™ 86xx-74xx, INTEL® x86, Freescale™ P1010, Coldfire®, Xilinx Zynq® SoC and Altera Cyclone5® SoC. We equip our boards with the most advanced memory subsystems and I/O controllers. When the availability of the system or the criticality of the applications are vital requirements we introduce our 2oo2 resource-sharing core (GeminiX2.0) optionally with our real-time operating system (GeminiX-OS) and other custom architectural improvements such as cross-channel data links.

NEAT manages a wide and ever-increasing hardware & software database containing complete design plans and documentation on previously developed single board computers, multi-board computers and complete systems. NEAT offers the customization of existing designs or for brand-new designs. Our design database and the fully equipped in-house laboratory permit us to meet short deadlines for “time-to-first-prototype”.

Light Railway Interlocking System
NEAT has experience in developing HW/SW SIL4 certified light railway Interlocking system for the management of trams in depots and on lines. The system is completed with a data preparation tool and automatic test system.

The system manages route requests (creation and cancellation) taking into account the feedbacks from the field elements (switch point machines, signals, track detectors, mass detectors, and axle counters). The system commands and controls the status of the field elements to safely manage the routes in each phase (from the creation to the completion) also in case of errors. Reset procedures are foreseen to manage and recover faulty situations caused by malfunctioning field elements or unexpected tram movements.

So far, our Light Railway Interlocking system has been installed in more than 20 different locations.

ERTMS/ETCS products
NEAT has experience in developing together with its clients:

- Generic Applications of an RBC according to the CENELEC EN 50128 SIL4 and Subset-026 requirements to achieve Level 2 and Level 3 Applications.
- A Generic Application and a Specific Application of a Radio Infill system according to CENELEC EN 50128 SIL4 and Subset-026 requirements. The Radio Infill Application manages level crossings and Infill extensions over multiple sections.
- Several communication plugins for Interlocking system based on Italian and European Standards (Subset-098, PVS).

ERTMS/ETCS protocols
NEAT and ERTMS Solutions have designed and developed a PVS library in ANSI C (MICRA compliant). NEAT provide support for integration and configuration of PVS Library inside client products (e.g. RBC or Interlocking).

NEAT provides support for ERTMS Solutions libraries:

- Subset-037 “ EuroRadio FIS” library: maintenance, integration inside client products and configuration.
- Subset-058 “FFFIS STM Application Layer” (including Subset-056 “STM FFFIS Safe time layer”, Subset-057 “STM FFFIS Safe link layer” and PROFIBUS libraries): maintenance, integration inside client products and configuration.
- Subset-098 “RBC-RBC Safe Communication Interface”.

Design and Configuration Tool for ERTMS
NEAT has developed a Tool that, starting from a CAD plan of the railway line:

- Allow the designer to check the coherence of the information in the railway schematic plan in several CAD format (i.e. AutoCAD and MicroStation).
- Extract information from CAD according to defined design rules.
- Calculate values for ERTMS variables in telegram.
- Produce Design output documents (AutoCAD and Excel format), Product configuration files (balise, encoder), and Test case data using standard open format (SUBSET-112 XML or RailML®).

The Tool is configurable to be able to manage CAD representation related to different markets. The tool is also able to import and export Subset-112 XML or RailML® files.
NEAT has developed in the last few years several Human Machine Interfaces (HMI) with high availability features and with safety integrity level, up to SIL3, based on the “composite fail safe paradigm”. A new version of the same HMI with safety integrity level up to SIL4 and adding the “reactive fail-safe paradigm” is currently in the prototyping phase.

Such HMIs are suitable for managing safety critical systems in railway applications as well as emergency systems in industrial plants.

Once the specific application requirements and the environmental requirements have been defined, NEAT selects the hardware components to use, either COTS or custom components (processors, input devices and LCDs). Dedicated HMI-Editor and Test Tool facilitate the design of the graphical interface of the HMI pages. The HMI-Editor has a plugin infrastructure capable of managing the configuration data of different HMI generic applications, including graphics and association of graphical objects and field entities.

NEAT has developed rugged, conduction cooled, single board computers for avionics and very high-performance computers for massive parallel computing. One of the most recent rugged computers for avionics is based on an x86 processor integrated with an AMD high performance GPU. NEAT managed the whole life cycle of this project, being in charge of the design, production and testing of the electronic system, of the development of the Board Support Package (BSP) and of the development of the first application. The electronic project includes standard interfaces (PCIe, Eth, USB, SATA, VGA) as well as custom interfaces: dedicated digital video out and custom bus. The BSP was entirely developed by NEAT including a BIOS and board specific drivers.

In the last two years NEAT has also developed a rugged custom board for space applications. This board has been specifically designed to control a particle detector for scientific purposes.

One of the most challenging and high performing computer systems recently designed by NEAT is a board for High Performance Computing & Networking (HPCN) applications. This board demonstrates NEAT’s know-how on the cutting edge of top technologies. It incorporates a multicore (8-cores) ARM® V8.64 CPU running at 2GHz with four independent DDR3 memory controllers (64b + ECC) handling a total amount of 32GB DDR3 memory soldered down into the board and running at 1666MHz. A huge set of high speed interfaces are available: two independent x8 PCI-express 3.0 ports, 4 SATA 3.0 ports, USB 2.0 and 3.0 ports, one SFP+ module with 10Gb Ethernet capability and a board management controller (allowing remote control of the board). These resources provide the user with unmatched calculus and hi-speed networking capabilities in a single low-power board.

NEAT has been a key member of the EC-funded FP7 “EUROSERVER” project, aiming at designing and prototyping technology, architecture, and systems software for the next generation of “Micro-Servers” to be used in building datacenters. NEAT is in charge of board design and development.

Moreover, NEAT is a member of the Shift2Rail founded “MOMIT” project, which aims at developing and demonstrating a new use of remote sensing technologies (satellite and remotely piloted aerial systems) for railway infrastructures monitoring. MOMIT solutions will mainly aim at supporting the maintenance and prevention processes within the infrastructure management lifecycle.
GeminiX SoC Reference Board is a highly integrated board implementing all the features of the new GeminiX2.0 platform leveraging the SoC technology, intended for the fast prototyping of SIL4 systems adopting GeminiX architecture and running GeminiX-OS and application software on the two local embedded CPUs.

GeminiX SoC Reference Board offers the following key features:

- GeminiX NODE-A (CPU-A plus CORE FPGA-A) collapsed into a Xilinx Zynq 7020 SoC
- GeminiX NODE-B (CPU-B and CORE FPGA-B) collapsed into an Altera Cyclone5 5CSEBA6 SoC
- Internal AXI 32b@100 MHz interface between CPU-A and GeminiX CORE-A
- Internal AXI 32b@100 MHz interface between CPU-B and GeminiX CORE-B
- 1kV (min) insulation between A & B galvanic areas (*)
- 3kV (min) insulation between A & B areas versus chassis (*)
- GeminiX interprocessor communication and synchronization channel
- Dedicated dual port RAM for high speed data exchange between NODE-A and NODE-B
- Cross channel data link implementing GeminiX redundancy features
- Internal voltage diagnostic
- Remote Power Supply Unit diagnostic
- 8kB NVRam
- 3x Ethernet 10/100 BASE-T per NODE-A
- 3x Ethernet 10/100 BASE-T per NODE-B
- 1x RS232 per NODE-A
- 1x RS232 per NODE-B
- 2x 16 bit I/O bus Interface for remote I/O boards
- -40°C ÷ +70°C operational (-40°C ÷ +85°C storage)
- Compliant with GeminiX-OS and GeminiX design flow

(*) Other insulation levels available on request
GeminiX core reference board is a rugged, highly integrated board implementing all the features of the GeminiX2.0 cores. The board is intended for the fast prototyping of SIL4 systems, adopting GeminiX architecture and running GeminiX-OS5 and application software on external CPUs with PCIe ports.

GeminiX Core Reference Board offers the following key features:

- PCIe gen2 x4 2GB/s from external COTS CPU-A
- PCIe gen2 x4 2GB/s from external COTS CPU-B
- 1.5kV (min) insulation between A & B galvanic areas
- 4.5kV (min) insulation between A & B areas versus chassis
- HW diversity:
  - Xilinx Artix7 FPGA implements GeminiX-Core for CPU-A
  - Altera CycloneV FPGA implements GeminiX-Core for CPU-B
- 1MB shared memory supporting GeminiX interprocessor communication and synchronization
- Cross channel data link implementing GeminiX redundancy features
- Internal voltage diagnostic
- Remote power diagnostic
- 8kB NVRam
- 2x Ethernet 10/100 BASE-T per CPU-A
- 2x Ethernet 10/100 BASE-T per CPU-B
- 2x RS232 per CPU-A
- 2x RS232 per CPU-B
- 8 bit I/O bus for remote I/O boards I/F (CPU-A)
- 8 bit I/O bus for remote I/O boards I/F (CPU-B)
- Fully conduction cooled: -40°C ÷ +70°C operational (-40°C ÷ +85°C storage)
GeminiX2.0 is the cutting-edge version of the first GeminiX HW/SW 2oo2 Platform. It is an embedded Virtual Platform for the realization of a safety critical system with a high SIL and implements base software and design hardware components that are independent of the final platform hardware. NEAT also offers the GeminiX Core Reference Board and the GeminiX SoC Reference Board, two rugged, highly integrated boards implementing all the features of the GeminiX2.0 Virtual Platform.

The GeminiX2.0 embedded Virtual Platform has been certified by ITALCERTIFER for development of SIL4 applications, being able to fulfill the safety requirements set by the CENELEC Standards EN 50126, EN 50128, EN 50129, EN 50159 and IEC 61508 up to SIL4. More than 20 different applications have been implemented using the GeminiX platform.

GeminiX2.0 consists of:
1. A Complete Platform Documentation Package and Application Conditions, which describe and certify the compliance for applications up to SIL4 according to the EN 50126/128/129 and IEC 61508 standards
2. A HW 2oo2 diverse architecture, supporting x2 for reliability
3. A real-time OS-like environment, GeminiX-OS, assessed as a SIL4 Generic Product by its own and also certified several times into clients’ products, independent from the specific hardware, including its own complete Documentation Package
4. A VHDL Source Code which implements diagnostic routines and generic I/O, independent from the specific hardware; several reference designs implemented using different CPUs (Intel, AMD, ARM, …) and different bus architectures

GeminiX facts:
- MISRA-C:2004, with coding rules and diagnostic coverage suitable for EN50128/IEC61508 up to SIL4
- Stand-alone self-booting executable
- Embedded safe configuration infrastructure
- Qualified on different CPUs: ARM®, Coldfire®, PowerPC™, x86
- Support for Lauterbach, Peedi, GDB and GHS debugging tools
- Test vectors for Vectorcast/C++™ testing tool included in verification kit
- Configurable isochronous interrupt service (resolution depending on CPU technology)
- Extremely low latency response for hard real time applications
- ARINC-653 APEX style Blackboard-based inter-process communication
- VHDL implemented core functionalities:
  - Passive memory protection
  - Power supply monitoring
  - Cross-communication (shared memories and synchronization)
  - DES acceleration engine
  - Watchdog with time-window
  - Internal buses diagnostic
- VHDL implemented I/O functionalities:
  - MAC core interface (MII)
  - GPIO controller
  - RS485/232/422 core
  - LED controller
  - Other custom I/O (e.g. Arinc 429, MIL-STD1553)
- The implementation of GeminiX is adopting the new System on Chip technology based on XILINX™ Zynq7000™ and ALTERA® CYCLONE® V devices.

Generic and Specific Applications
A typical Generic Application built on top of GeminiX-OS should provide custom I/O handler (possibly with their own protocols) and logic managers as well as baseline configuration data, to be augmented with those of the Specific Application for final deployment machine.

Generic Application may be developed “by-hand” or using Model Driven Development (by inserting defensive programming measures into MathWorks Matlab generated code with TargetIT, or by using ANSYS® SCADE Suite®).

Design flow and documentation package
GeminiX hardware and SW products are designed to reduce the development time of clients’ SIL4 systems.
They include a fully featured documentation package, from hazard analysis down to hardware reference designs and software source code with their validation kits.
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